

WHAT IS CLAIMED IS:

1. A method for controlling delay over process, supply-voltage, and temperature variations, comprising:

- (1) receiving a waveform;
- (2) delaying said waveform;
- (3) outputting said delayed waveform to an output terminal using at least one relatively low-power driver transistor;
- (4) providing supplemental output drive to said output terminal after an unexpected period of delay, using at least one relatively high-power driver transistor;
- (5) sensing a level of said delayed waveform; and
- (6) preventing said supplemental output drive from being reduced as said sensed level falls below a threshold.

2. The method according to claim 1, wherein said step (5) comprises sensing a voltage level.

3. The method according to claim 1, wherein said step (5) comprises sensing a current level.

4. The method according to claim 1, wherein said steps (1)-(5) are performed for rising edge and falling edge portions of the waveform.

5. The method according to claim 1, wherein said at least one relatively low-power driver transistor includes at least one PMOS transistor and at least one NMOS transistor.

6. The method according to claim 1, wherein said at least one relatively high-power driver transistor includes at least one PMOS transistor and at least one NMOS transistor.

7. The method according to claim 1, wherein:

said step (2) includes performing a plurality of serial delay operations, including at least one initial delay operation and a final delay operation, on said waveform;

said step (4) includes providing supplemental output drive to said output terminal through one or more compensation-path delay elements; and

said step (5) includes sensing a level of said delayed waveform output from one of said initial delay operations.

8. An apparatus for controlling delay over process, supply-voltage, and temperature variations, comprising:

means for delaying a waveform;

means for outputting said delayed waveform to an output terminal using at least one relatively low-power transistor;

means for providing supplemental output drive to said output terminal after an unexpected period of delay, using at least one relatively high-power driver transistor;

means for sensing a level of said delayed waveform; and

means for preventing said supplemental output drive from being reduced as said sensed level falls below a threshold.

9. An apparatus for controlling delay over process, supply-voltage, and temperature variations, comprising:

an input terminal;

an output terminal;

a first path coupled between said input terminal and said output terminal, said first path including at least one relatively low-power output driver transistor that outputs a delayed representation of a received waveform to said output terminal;

a second path coupled between said input terminal and said output terminal, said second path including at least one relatively high-power output driver transistor that outputs said delayed representation of a received waveform to said output terminal, said second path including a disabling circuit;

a feedback path including a sensing circuit coupled to an output of said first path, said feedback path including an output coupled to said second path disabling circuit, wherein said feedback path outputs a feedback signal to said disabling circuit that increasingly disables said at least one relatively high-power output driver as a waveform output from said first path rises above a threshold; and

a feedback prevention path coupled between the output of said at least one relatively low-power output driver transistor and a gate terminal of an NMOS device, wherein as said waveform output from a first of said relatively low-power output driver transistor falls, said NMOS device prevents said disabling circuit from disabling said at least one relatively high-power output driver.

10. The apparatus according to claim 9, wherein said at least one relatively low-power output driver transistor comprises an inverter.